Impact of nitrogen annealing on the performance of SiON based nano-MOS employing bi-layer metal gate

Richa Gupta* and Rakesh Vaid

Department of Physics & Electronics,
University of Jammu, Jammu-180006, J&K, India.
*Corresponding author: 1richagupta@gmail.com

Abstract: This paper investigates the impact of nitrogen annealing on the performance of Silicon Oxynitride as gate insulator. For this study, we fabricated two sets of metal-insulator-semiconductor (MIS) structures: Pt-Ti/As-deposited SiON/n-Si and Pt-Ti/N_2 annealed/SiON/n-Si. SiON film (~10nm) was grown using 2-inch general purpose anneal furnace followed by the rapid thermal annealing at 500^0C in nitrogen ambient. The electrical characterizations of the fabricated structure were studied using capacitance-voltage (C-V) and current-density versus voltage (J-V) measurements. The physical characterization involves atomic force microscopy (AFM) and Fourier transform infrared spectroscopy (FT-IR). Annealing in nitrogen ambient resulted in capacitance increase and hence improved the performance parameters of the fabricated structure. Moreover, an excellent suppression in leakage current density is the outcome of significant amount of nitrogen incorporated into the SiON film.

Keywords: Silicon Oxynitride (SiON); dielectric constant; effective oxide thickness (EOT).

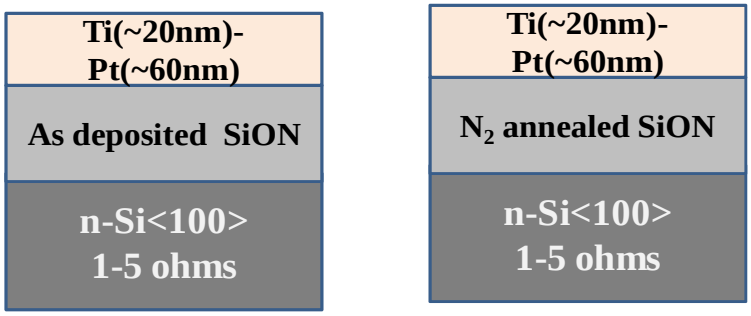
1. Introduction

For more than 40 years, SiO_2 has been used as gate dielectric because of its manufacturability and ability to improve the transistor performance [1,2]. However, incremental improvements in CMOS processing has uncovered the limitations of the SiO_2 gate dielectrics over the silicon industry [3,4]. To improve MOS transistor performance in the past, chip manufacturers have tried to shrunk the thickness of the gate dielectric to about 1.2 nm. Although this has helped transistors to gain high speeds, the problem is that the very thin layers of SiO_2 suffers from leakage current, resulting in energy wastage and heat dissipation. Moreover, reliability also becomes a huge concern for a very thin layer SiO_2 film. Oxynitride based gate dielectrics have been considered as alternative gate dielectrics for the 65nm CMOS technology and even beyond to replace conventional SiO_2. The segregation of nitrogen atoms at the Si-SiO_2 interface has shown to improve the reliability of MOSFETS. Oxynitride has shown improved electrical characteristics, such as reduced interface state generation and also deactivates the phenomenon of dopant diffusion. Various techniques have been developed to incorporate nitrogen into SiO_2 [5]. Oxynitrides can be formed by one of the following methods: (a) nitridation of SiO_2 by ammonia, nitrous oxide (N_2O) or nitric oxide (NO), (b) simultaneous nitridation and oxidation of Si surface with N_2O and NO, (c) ion implantation of N_2 into the Si surface followed by oxidation and (d) N_2O remote plasma-assisted oxidation/nitridation of the Si surface.

In this work, we have used a novel method for growth of SiON film. 2-inch annealing furnace was used for oxynitride growth having N_2O gas flow at 1000^0C, followed by rapid thermal annealing in nitrogen ambient.

2. Experimental Details

Two sets of fabricated MOS capacitors are illustrated by Figure 1. Single side polished (SSP) n-type Si <100> substrates having a resistivity of 1-5 Ω cm were chemically cleaned by the standard RCA method. SiON film ~ 10nm was grown using 2-inch annealing furnace having 1000 Sccm N_2O gas flow at temperature of 1000^0C for 15 minutes. After that one set of MOS capacitor was taken as a dummy sample and the second one was annealed by RTP Annealsys AS-ONE system in nitrogen ambient at 500^0C. The thickness of grown SiON film was confirmed by Ellipsometry measurements. For the top gate electrode, 1000 ̊A thick layer with Ti = 20nm and Pt = 60nm was deposited by 4 target E-beam evaporator system over a circular area of 18 $\times 10^{-4}$ cm^2 through a shadow mask. To remove the native oxide on the back side, etching was performed by buffered hydrofluoric acid (BHF) followed by rinsing in de-ionized water.



(a) (b)

Figure 1: Fabricated structures: (a) Pt-Ti/As deposited SiON/n-Si and (b) Pt-Ti/N_2 annealed SiON/n-Si

On the back side of silicon wafer, Aluminum film was deposited for making back contact. Finally, Post metallization annealing (PMA) was performed at 420 °C for 20 minutes using forming gas (96%N_2, 4%H_2) ambient. To extract the various performance parameters, the measurements of the fabricated device were carried out using Keithley 4200-SCS at room temperature under dark conditions.

3. Physical Characterization

3.1 Atomic Force Microscopy (AFM)

AFM is one of the most feasible methods to calculate the roughness of a sample surface at a high resolution. Moreover, this method distinguishes the sample based on its mechanical properties such as - hardness and roughness. Figure 2 (a) and 2 (b) represents the atomic force measurement of as-deposited and N_2 annealed SiON films respectively. The surface roughness for as-deposited SiON film was found to be 0.3526 nm. However, for the nitrogen annealed SiON film, the r.m.s. value of about 0.2265 nm was observed. This indicates that nitrogen annealing plays a significant role in reducing the roughness of sample surface. Infact, the morphology of oxynitride film exhibited the excellent film quality.

3.2 Fourier Transform Infra-red spectroscopy (FTIR)

Figure 3 represents the FT-IR spectra of the SiON film. To reflect the absorbance of the grown film, infrared absorption spectra of the bare-Silicon wafer was used as background spectra and finally

subtracted from the total spectrum. The IR spectrum of the grown SiON film at 1000^0C temperature lies in the range of 500 cm^{-1} to 3500 cm^{-1} wave numbers. Si-O-Si asymmetrical stretching mode is exhibited by the first significant band assigned at 1072 cm^{-1} [6,7] while band at 886 cm^{-1} is associated with Si-N-Si stretching [8]. It is interesting to note that the bonds at 3325 cm^{-1} are associated with the N–H stretching mode and is the clear detection of the presence of nitrogen [9]. The bonds at 2584 cm^{-1} corresponds to Si-H stretching [10] whereas 2918 cm^{-1} reflects the Si-OH stretching. A narrow peak at 3325.24 cm^{-1} indicates the presence of N-H stretching, which is basically the hydrogen concentration in the film.

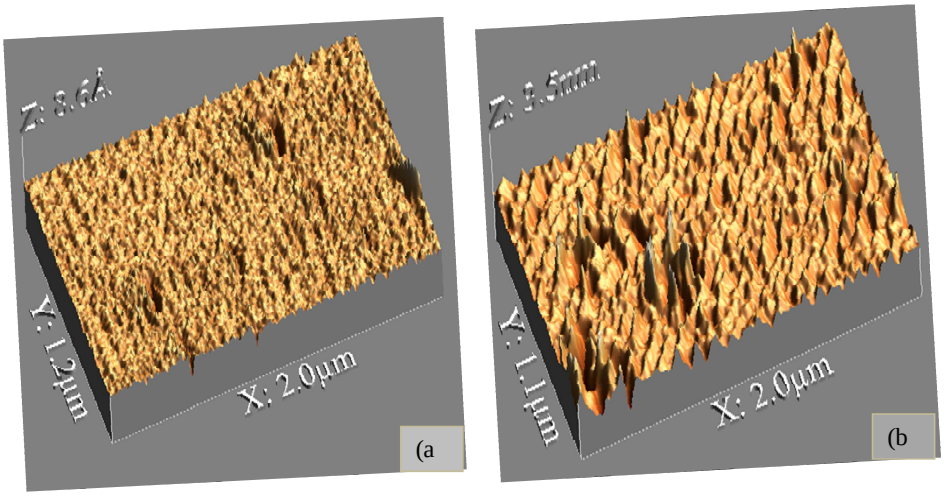


Figure 2: 3-D AFM image of (a) As-deposited SiON and (b) N_2 annealed SiON having 2 ×2 µm scanning

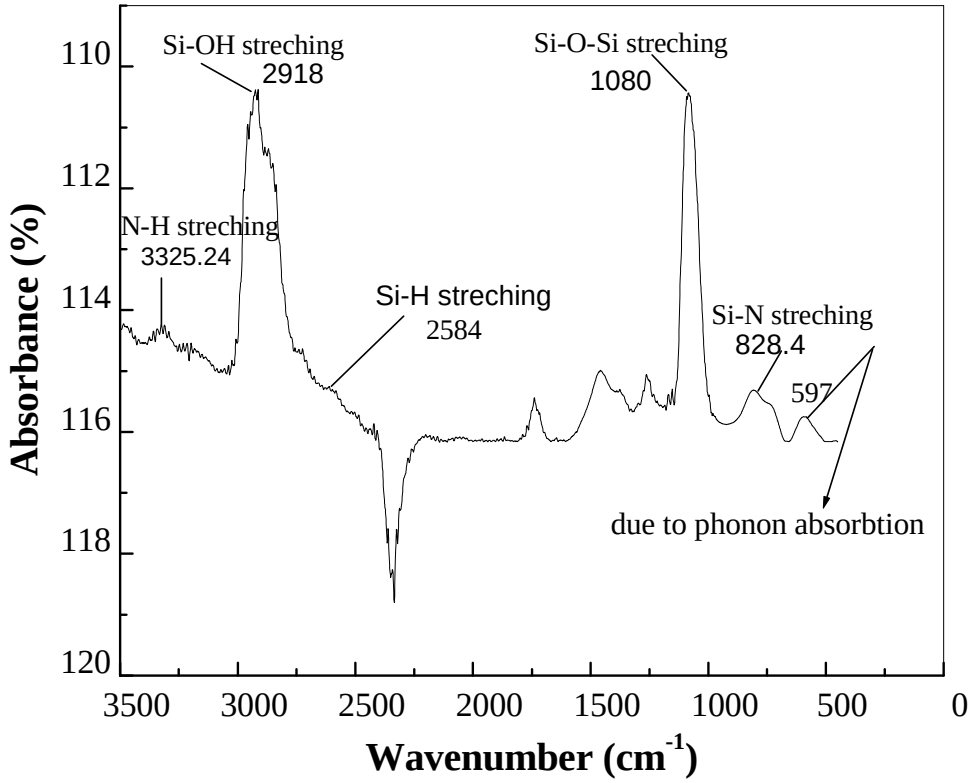


Figure 3: FTIR spectra of SiON film

4. Electrical Characterization

In this section, we shall discuss the electrical characterization of the fabricated MOS-capacitors such as C-V and J-V curves and finally the calculation of performance parameters from these curves.

4.1 Capacitance versus Voltage (C-V) analysis

Figure 4 (a) and 4(b) shows the C-V curves of the as-deposited and N_2 annealed SiON based MOScaps at 100KHZ and 500KHZ respectively. The C-V curves of as-deposited SiON films are almost the same as there of the N_2 annealed SiON film due to the annealing effect. C-V shift indicates an increase in oxide fixed charges. However, it is quite interesting to note that there is increase in capacitance for N_2 annealed SiON film indicating that the percentage of traps at the interface strongly depends on the incorporation of nitrogen. At accumulation and depletion region, the measured values of capacitance decreases with the increasing frequency. This clearly reveals the presence of the localized interface states at the interface.

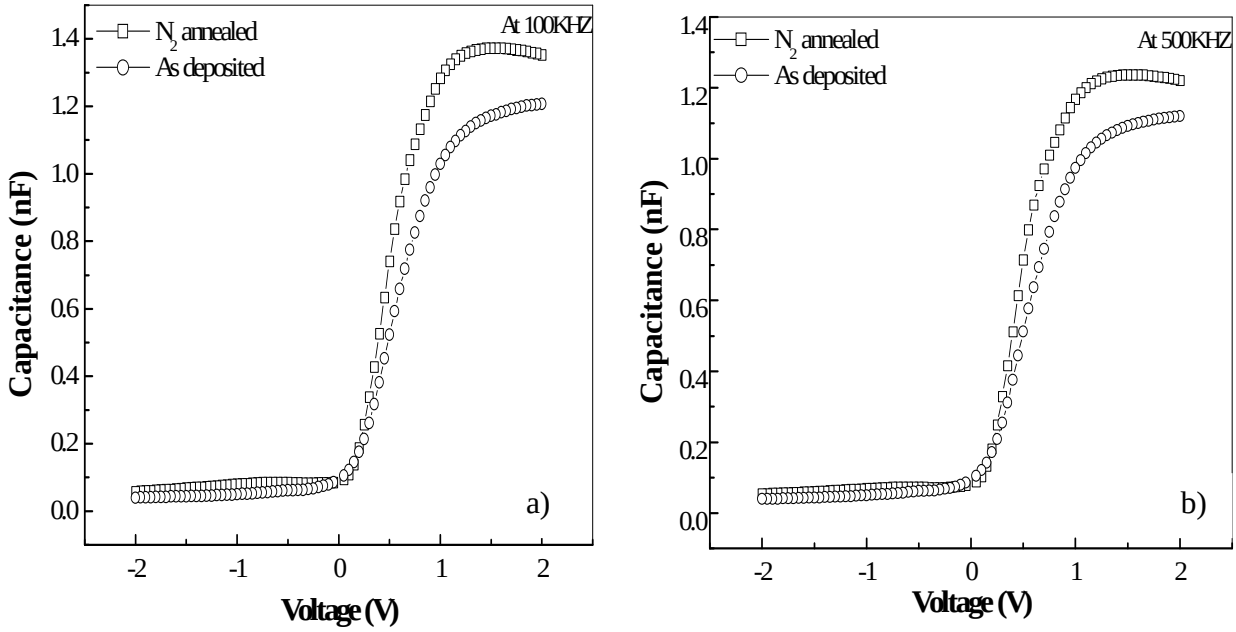


Figure 4: C-V characteristics of Pt-Ti/SiON/n-Si at (a) 100 KHz and (b) 500 KHz

From the C-V curves, various parameters have been extracted such as dielectric constant, effective oxide thickness and effective oxide charge. All the calculations have been performed at 500KHZ. The computed parameters have been given in Table 1. The achieved dielectric constant (k) of SiON films was extracted from the accumulation region of C-V curve using the equation (1):

$$K = \left(C_{acc} \times t_{ox}\right) \Big/ \left(A \times \varepsilon_0\right) \tag{1}$$

where, C_{acc} is the maximum value of accumulation capacitance, t_{ox} is the thickness of SiON film i.e. T_{SiON} = 10nm, A is the Ti-Pt gate electrode area and ε_o is the permittivity of free space. In the C-V curve, flat band voltage (V_{fb}) has shifted towards the positive voltage indicating the existence of oxide charge in the SiON/Si interface. The effective oxide charge Q_{eff} was calculated from the C-V curve based on the following equation [11].

$$Q_{eff} = {(\Delta V_{fb} \times C_{ox})}/{(q \times A)} \quad (2)$$

where, ΔV_{fb} is the flat band voltage shift, C_{ox} is the oxide capacitance and q is the electronic charge.

Table 1: Parameters extracted from C-V curve of Pt-Ti/SiON/n-Si at 500KHZ

Process Variations	Dielectric Constant (K)	Effective oxide thickness (EOT in nm)	Effective oxide charge (Q_{eff} in Cm^{-2})
As deposited SiON	6.9	5.6	0.33×10^{14}
N_2 annealed SiON at 500^0C	7.3	5.3	0.33×10^{15}

4.2 Current density versus voltage (J-V) measurement

The leakage current density (J) of as-deposited and N_2 annealed oxynitride based nano-MOS was measured as a function of voltage as shown by Figure 5. The leakage current density at -1V for as-deposited and N_2 annealed SiON film was found to be 1.6×10^{-6}A/cm^2 and 3.8×10^{-9}A/cm^2 respectively. The nitrogen annealed SiON film has effectively reduced the defects present at the interface of Si/SiON stack. This means that the good percentage of nitrogen has been segregated by RTP at 500^0C.

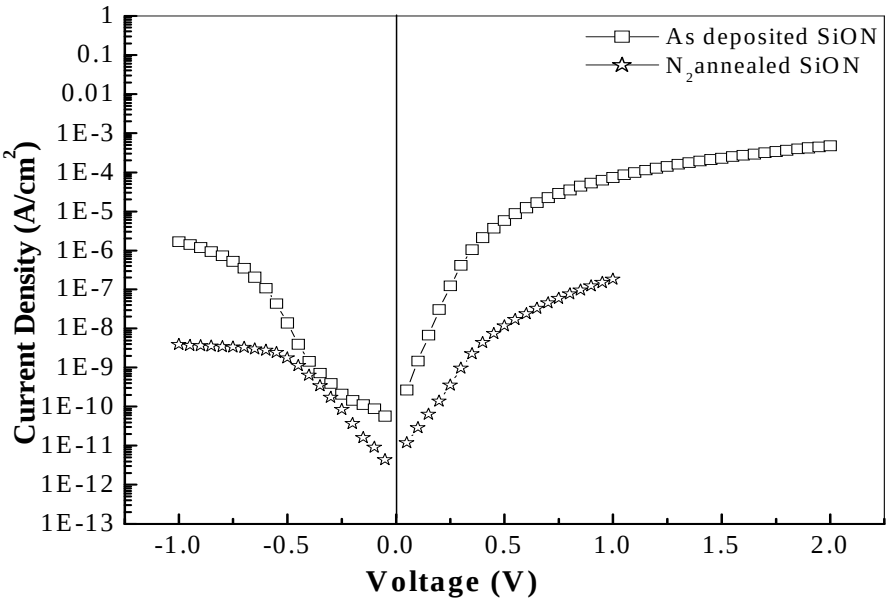


Figure 5: J-V characteristics of Pt-Ti/SiON/n-Si at room temperature

5. Conclusions

We successfully fabricated Ti-Pt/SiON~10nm/n-Si nano-MOS with achieved dielectric constant ~ 7.3 for N_2 annealed SiON. AFM studies confirms that the smoothness of grown films. The value of EOT for N_2 annealed film has reduced to about 5.3nm. Moreover, a remarkable decrease in the interface trap density was observed owing to the rapid thermal annealing in nitrogen ambient. Such a progress in device scaling is the doorway to power saving.

6. Acknowledgements

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