Study of transient characteristics of XNOR gate using FGMOS and QFGMOS

Roshani Gupta*, Rockey Gupta and Susheel Sharma

Department of Physics & Electronics,
University of Jammu, Jammu-180006, India
*Corresponding author: roshani24gupta@gmail.com

Abstract: This paper presents the design of XNOR gate using quasi-floating-gate MOSFET (QFGMOS) and highlights its advantages over FGMOS and CMOS based XNOR gates. The comparative transient analysis of CMOS, FGMOS and QFGMOS based XNOR gates with regard to different design parameters such as propagation delay and energy delay product has been carried out. From the simulation results it has been observed that QFGMOS based XNOR gate exhibits lower values of propagation delay and energy delay product as compared to its FGMOS and CMOS versions. The workability of these circuits has been verified through PSpice simulations carried out using level 7 parameters in 0.13 µm CMOS technology with a supply voltage of 1 V.

Keywords: Quasi-Floating-gate MOSFET; CMOS; XNOR gate; transient characteristics.

1. Introduction

Lowering power supply voltage is the most efficient method to reduce power dissipation and raise system reliability [1-3]. Some of the low voltage techniques used to reduce supply voltages are level shifters, self-cascode MOSFETs, sub-threshold MOSFETs, bulk-driven MOSFETs, and floating gate MOSFETs (FGMOS). Out of these FGMOS presents a unique advantage of programmability of threshold voltage, which can be lowered from its conventional value, thus makes it suitable for low voltage applications. FGMOS is compatible with standard double-poly CMOS process technology and has been used to develop digital-to-analog (D/A) and analog-to-digital (A/D) converters, resistors, electronic programming, neural networks, and operational transconductance amplifier, etc [4-6]. Though we can alter the effective threshold voltage as seen from one of the n-inputs to have a lower threshold voltage for low voltage applications, but there are some limiting issues with multi-input floating-gate structures. To change the threshold voltage we require complex programming circuitry and higher programming voltage, thus defeating the purpose of a low-voltage design [7]. Also, the large input coupling capacitance leads to an increase in silicon area and reduction of the circuit's effective transconductance and gain-bandwidth product. These limitations are overcome in the modified structure of FGMOS known as Quasi-floating-gate MOSFET (QFGMOS) [8, 9].

In this paper, we have employed quasi floating-gate MOSFET (QFGMOS) to implement XNOR gate and compared its performance with its FGMOS and CMOS counterpart. The performance of these circuits has been verified through PSpice simulations carried out using level 7 parameters in 0.13 µm CMOS technology with supply voltage of 1V.

2. Quasi Floating-Gate MOSFET

The Quasi floating-gate MOSFET is very similar to the floating-gate MOSFET, however, the gate is not left floating at dc. Instead a large valued resistor implemented through a reverse-biased MOSFET

is attached to the gate of the transistor and then connected to one of the power supplies. Fig. 1 shows the equivalent circuit representation of an N-input n-channel QFGMOS transistor [9-11].

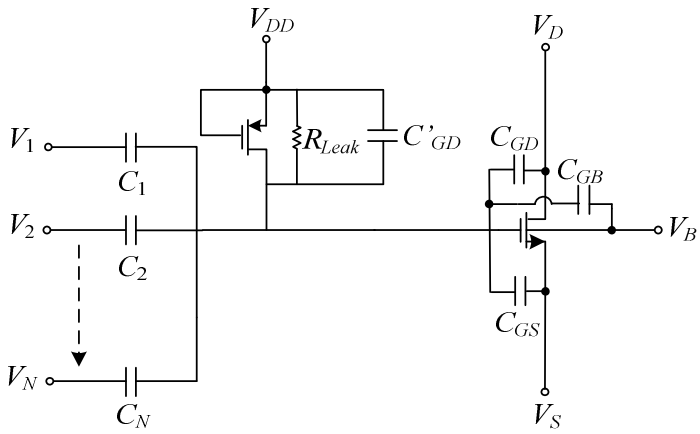

Figure 1: Quasi floating gate MOSFET

3. XNOR Gate using FGMOS

The circuit of FGMOS XNOR gate is shown in Fig. 2. It is similar to that of CMOS XNOR gate except that extra capacitances are introduced between the conventional gate and the input signal gate. The bias voltages V_{bp} and V_{bn} provide tunability to the threshold voltages of p and n-channel FGMOS respectively.

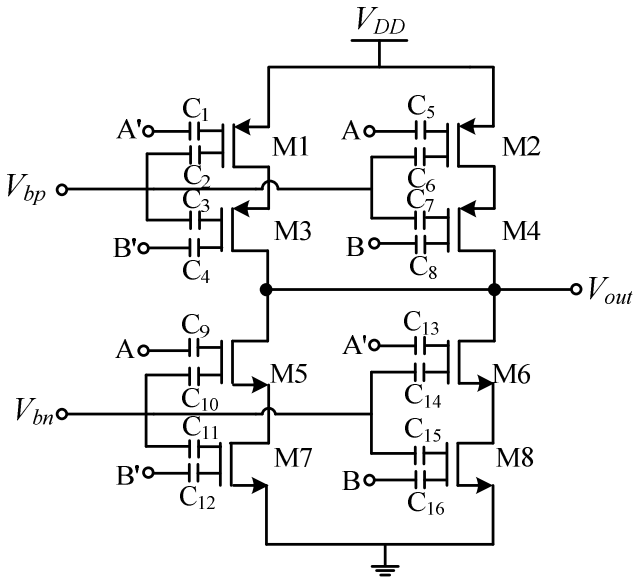

Figure 2: XNOR gate using FGMOS

The performance of FGMOS XNOR gate can be characterized through its transient characteristics which is a plot of input and output voltage with respect to time [12, 13]. The simulation of circuit shown in Fig. 2 has been performed to obtain its transient response at different values of V_{bp} and V_{bn} with supply voltage of 1 V and is shown in Figs. 3 and 4 respectively. In Fig. 3, bias voltage of p-channel FGMOS transistors (V_{bp}) is varied from 0 V to 1 V, while keeping bias voltage of n-channel FGMOS transistors (V_{bn}) fixed at 1 V. Similarly in Fig. 4, V_{bn} is varied from 0 V to 1 V, while keeping V_{bp} fixed at 0 V and output voltage (V_{out}) is obtained with respect to time.

Figure 3: Transient response of XNOR gate using FGMOS at different V_{bp}

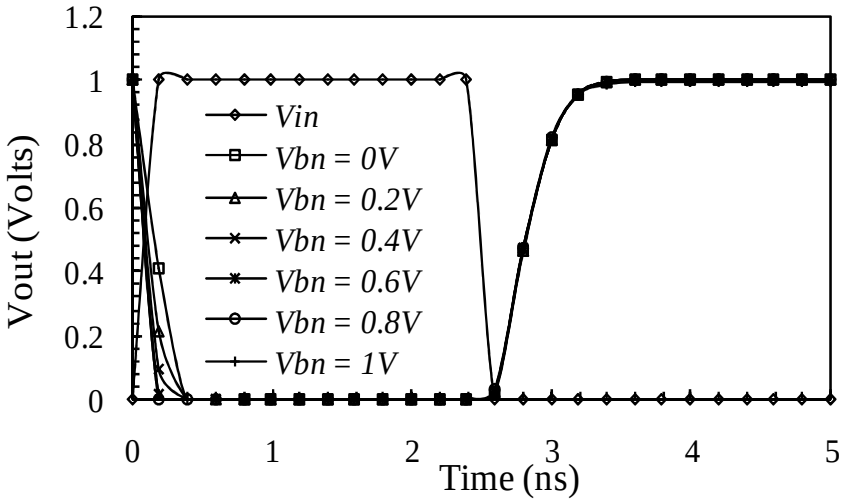

Figure 4: Transient response of XNOR gate using FGMOS at different V_{bn}

Now, from the transient responses shown in Figs. 3 and 4, we have calculated the propagation delay at different values of bias voltage as shown in Figs. 5 and 6 respectively.

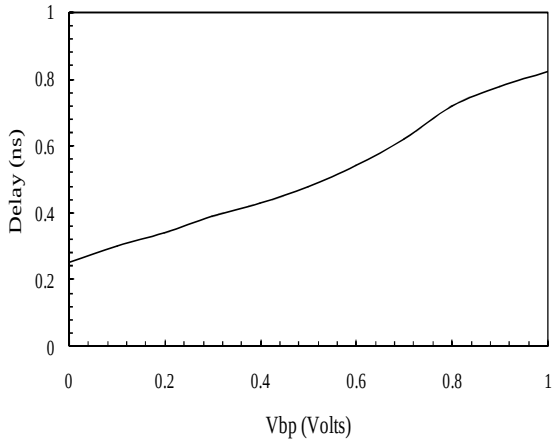

Figure 5: Propagation delay at different values of V_{bp}

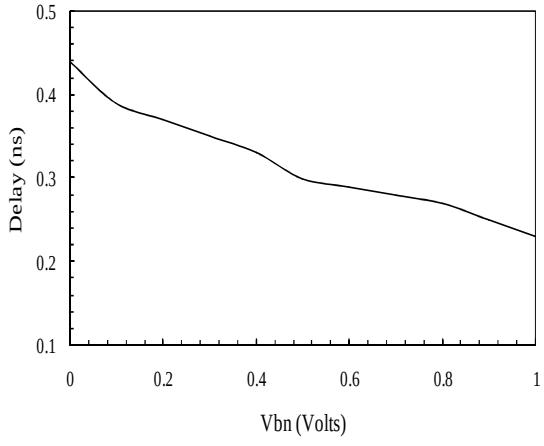

Figure 6: Propagation delay at different values of V_{bn}

The variation of propagation delay at different values of V_{bp} and V_{bn} is presented in Table 1.

Table 1. Effect of bias voltage on propagation delay

V_{bp} (Volts)	Delay (ns)	V_{bn} (Volts)	Delay (ns)
0	0.25	0	0.44
0.2	0.34	0.2	0.37
0.4	0.43	0.4	0.33
0.6	0.54	0.6	0.29
0.8	0.72	0.8	0.27
1.0	0.82	1.0	0.23

From the above results, it has been found that as we go on increasing the bias voltage of p-channel FGMOS transistor from 0 V to 1 V, propagation delay increases from 0.25 ns to 0.82 ns, where as increasing bias voltage of n-channel FGMOS transistor from 0 V to 1 V reduces propagation delay from 0.44 ns to 0.23 ns. Therefore, by selecting bias voltages of p and n-channel FGMOS at 0 V and 1 V, propagation delay can be minimized, thus enhancing the operating speed.

4. XNOR Gate using QFGMOS

In order to enhance the performance of XNOR gate, it is important to minimize the propagation delay [14, 15]. The propagation delay of XNOR gate can be reduced by implementing the circuit of XNOR gate using quasi-floating-gate MOS transistor as shown in Fig. 7.

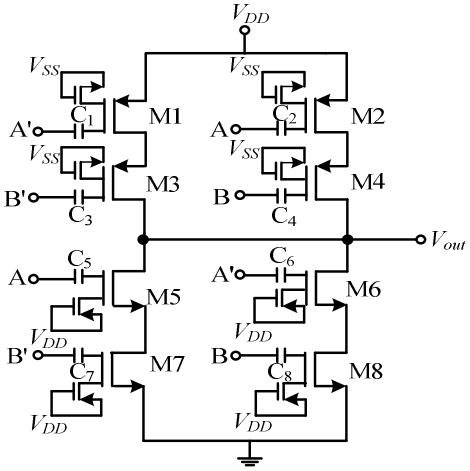

Figure 7: XNOR gate using QFGMOS

The circuit of QFGMOS XNOR gate has been simulated to obtain its transient characteristics by selecting *W/L* of M1, M2, M3 and M4 as 2.6 μm/0.13 μm and M5, M6, M7 and M8 as 1.3 μm/0.13 μm with supply voltage of 1 V. The simulation results are shown in Fig. 8

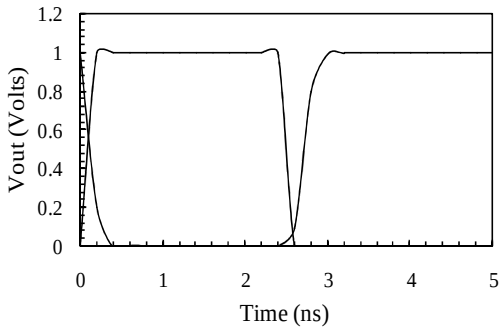

Figure 8: Transient characteristics of QFGMOS XNOR gate

Now, the comparative transient characteristics of XNOR gate using CMOS, FGMOS and QFGMOS have been obtained by selecting bias voltages of p and n-channel FGMOS transistors fixed i.e. V_{bp} = 0 V and V_{bn} = 1 V with supply voltage of 1 V and are shown in Fig. 9. It has been found that QFGMOS based XNOR gate has propagation delay of 0.12 ns which is less as compared to FGMOS (0.23 ns) and CMOS XNOR gate (0.33 ns).

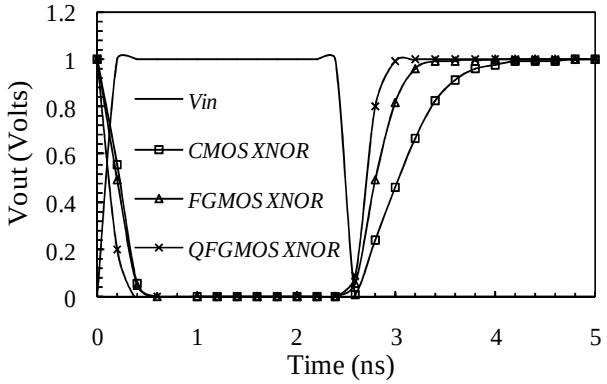

Figure 9: Comparative transient response of XNOR gate

Now, the values of propagation delay obtained from the transient response of XNOR gate using CMOS, FGMOS and QFGMOS has been used to calculate the energy delay product (EDP) at different values of supply voltage (V_{DD}). The comparative EDPs of CMOS, FGMOS and QFGMOS XNOR gate is shown in Fig. 10.

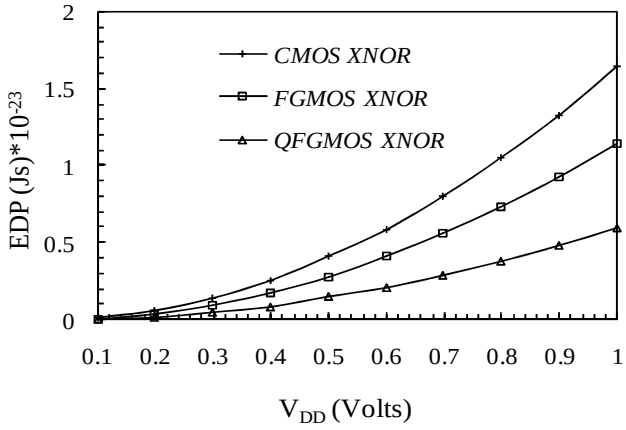

Figure 10: Comparative EDPs of XNOR gate

From the graph in Fig. 10, it has been found that energy delay product varies with supply voltage and for V_{DD} =1V, the value of EDP for QFGMOS XNOR gate is 0.6×10^{-23}Js as compared to FGMOS (1.15×10^{-23}Js) and CMOS XNOR gate (1.65×10^{-23}Js). Therefore, XNOR gate designed using QFGMOS is better since the energy delay product is lower than FGMOS and CMOS XNOR gate.

5. Conclusion

In this paper, we have discussed the transient characteristics of XNOR gate using CMOS, FGMOS as well as QFGMOS. The performance of QFGMOS based XNOR gate has been compared with its FGMOS and CMOS versions. We have observed that XNOR gate designed using QFGMOS results in less propagation delay and energy delay product as compared to FGMOS and CMOS XNOR gate. The performance of these circuits has been verified through PSpice simulations carried out using level 7 parameters in 0.13 µm CMOS technology with a supply voltage of 1 V.

References

[1] Chandrakasan, A. P., Sheng, S., Brodersen, R. W., Low-Power CMOS Digital Design. IEEE Journal of Solid-State circuits, **27** (**4**), 473-484 (1992).

[2] Gonzalez, R., Gordon, B. M., Horowitz, M. A., Supply and Threshold Voltage Scaling for Low Power CMOS. IEEE Journal of Solid-State circuits, **32** (**8**), 1210-1216 (1997).

[3] Yan, S., Sinencio, E. S., Low voltage analog circuit design techniques: A Tutorial. *IEICE* Trans. Fundamentals, **E00-A** (**2**), 1-17 (2000).

[4] Pandey R., Gupta, M., FGMOS based Voltage-Controlled Grounded Resistor. Radioengineering, **19** (**3**), 455-459 (2010).

[5] Keles, S., Kuntman, H. H., Four Quadrant FGMOS Multiplier. Proceedings of ELECO'2009: The 6th International Conference on Electrical and Electronics Engineering, **2**, 45–48 (2009).

[6] Murthy, P.H.S.T., Chaitanya, K., Krishna M. M., Rao.V, M., FTL based 4Stage CLA Adder Design with Floating Gates. International Journal of Computer Applications, **17** (**6**), 1-5 (2011).

[7] Khateb, F., Khatib, N., Kubanek, D., Low voltage ultra low power current conveyor based on quasi- floating gate transistors. Radio engineering, **21** (**2**), 725-735 (2012).

[8] Seo, I., Fox, R. M., Comparison of Quasi-/Pseudo-Floating Gate Techniques and Low-Voltage Applications. Analog Integrated circuits and Signal Processing, **47**, 183-192 (2006).

[9] Angulo, J. R., Lopez-Martin, A. J., Carvajal, R. G., Chavero, F. M., Very Low-Voltage Analog Signal Processing Based on Quasi Floating Gate Transistors. IEEE Trans. Solid-State Circuit, **39** (**3**), 434-442 (2004).

[10] Angulo, J. R., Urquidi, C. A., Carvajal, R. G., Torralba, A., Martin, A. L., A new family of very low-voltage analog circuits based on quasi-floating-gate transistors. IEEE Trans. Circuits Syst. II, **50**, 214-220 (2003).

[11] Algueta Miguel, J. M., Lopez Martin, A. J., Acosta, L., Angulo, J. R., Carvajal, R. G., Using floating gate and quasi floating-gate techniques for rail to rail tunable CMOS transconductor design. IEEE Trans. Circuits and Systems I, **58** (**7**), 1604-1614 (2011)

[12] Hodges, D. A., Jackson, H. G., & Saleh, R. A. (2005). Analysis and Design of Digital Integrated circuits. MC Graw-Hill.

[13] Razavi, B. (2008). Fundamentals of Microelectronics. John Wiley and sons.

[14] Rabaey, J., Chandrakasan, A., & Nikolic, B. (2003). Digital Integrated circuits. A Design Perspective, Prentice Hall.

[15] Uyemura, J. P., (2002). Introduction to VLSI circuits and systems. John Wiley and sons, New Delhi. 2002.